

ARSLAN ALI

📞 +1 647-470-2844 ✉ arslan.ali0161@gmail.com  [Arslan Ali](#)  [arslanalia](#)  [arslanali.vercel.app](#)

Education

Toronto Metropolitan University (Formerly Ryerson University)

September 2023 – April 2028

Bachelor of Engineering in Electrical Engineering

Toronto, ON

- Relevant Coursework: Electronic Circuits, Microprocessor Systems, Data Structures and Algorithms

Technical Skills

Languages: Python, Java, C, HTML/CSS, MATLAB, VHDL

Technologies/Frameworks: MultiSim SPICE, Quartus, Linux, Git, Cisco IOS, Excel

Tools: Multimeters, Oscilloscopes, Function Generators, FPGA Development Boards, Arduino, Breadboard

Certifications: Cisco Certified Network Associate (CCNA)

Experience

Software Developer

March 2025 – May 2025

Happy Nutrition

Toronto, ON

- Led development of an AI-powered health advisor by integrating a Large Language Model into a web application, enabling personalized nutrition guidance and increasing user engagement by approximately 30% during user testing.
- Designed and deployed containerized backend services using Docker, and collaborated through GitHub for version control and file sharing, ensuring consistent development environments and smooth team coordination.
- Collaborated in a team of six, taking ownership of the AI integration pipeline while contributing to the development of the website, online store, and student dashboard using HTML, JavaScript, and Tailwind CSS, improving overall platform usability and workflow efficiency.
- Implemented client-side logic and API integration in JavaScript, connecting frontend components to AI services and delivering a responsive, modern user interface.

Design Engineer

April 2023 – August 2023

TMAV

Toronto, ON

- Contributed to the development of a Python-based time-of-flight simulation tool that evaluated motor–battery power requirements and total energy consumption using motor test data and battery constraints to compare system configurations and reduce reliance on repeated physical flight testing.
- Performed electrical analysis involving battery capacity, maximum current draw limits, and electrical power consumption, supporting estimation of net energy usage during climb, cruise, and descent operating phases.
- Assisted with analyzing experimental data to relate thrust and electrical power, applying curve fitting techniques that improved agreement between modelled and measured results by 15%.
- Supported the use of decision matrices to prioritize electrical and energy-related factors affecting time of flight, contributing to iterative improvements of the simulation workflow.

Projects

Multi-Stage BJT Amplifier | *Analog Circuits, SPICE*

April 2025

- Designed a multi-stage BJT amplifier to achieve a specified voltage gain while meeting constraints on available components and operating conditions.
- Performed theoretical analysis of BJT operation and biasing to develop the circuit design, and validated performance using MultiSim SPICE simulation.
- Evaluated amplifier performance under loaded and unloaded conditions, achieving measured gain within 2.8% of the target value across all test scenarios.

Space Weather Prediction App | *Python, NASA DONKI API, Machine Learning*

January 2025

- Developed a Python application that retrieves and processes real-time space weather data from NASA's DONKI API, analyzing solar flares, geomagnetic storms, CMEs, SEPs, and interplanetary shocks.
- Trained a Random Forest model on 10 years of historical NASA data to predict future solar flare intensity classes and time-to-event, achieving 78% classification accuracy and a 1.67-day average prediction error.
- Engineered a 10-dimensional feature set incorporating temporal attributes, event intensity, duration, and historical lag to improve predictive performance.

General-Purpose Processor Design | *VHDL, FPGA, Digital Systems*

December 2024

- Designed and implemented an 8-bit Arithmetic Logic Unit (ALU) and control unit in VHDL, simulating functionality in Quartus II and validating the design on an FPGA development board.
- Developed modular and hierarchical VHDL code for the ALU, control logic, and I/O registers, ensuring clear signal flow, maintainability, and correct sequencing of operations.
- Implemented an FPGA output interface using dual 7-segment displays, converting 8-bit binary results to hexadecimal format and optimizing control logic to reduce combinational delay.